ABSTRACT

A method for fabricating a capacitor with overlying transistor without stress-induced voids is described. A capacitor stack is provided overlying a substrate. A stress-balancing dielectric layer is deposited overlying the stack. An anti-reflective coating (ARC) layer is deposited overlying the stress-balancing layer. The stack is patterned to form the capacitors. Gate transistors are formed overlying the capacitors wherein the stress-balancing layer prevents formation of stress-induced voids during the thermal processes involved in forming the gate transistors.